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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,906	06/26/2001	Robert J. Proebsting	5646-54	1428

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EXAMINER	
NGUYEN, DANNY	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 01/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,906	PROEBSTING, ROBERT J.	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The indicated allowability of claims 3, 8-12, and 15 are withdrawn in view of the newly discovered reference(s) to Drapkin et al (USPN 6,400,546) and Partovi et al (USPN 6,281,713) Rejections based on the newly cited reference(s) follow.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 4, 13, and 20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 4, 5, 7, 20-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Drapkin et al (USPN 6,400,546).

Regarding to claim 1, Drapkin et al discloses an over-voltage protection circuit (fig. 2 and 3) comprises a pass transistor (e.g. transistor 234) having a first and a second current carrying terminals electrically connected to an input (e.g. supply voltage 104) and an output signal line (such as at output node 114) respectively, a voltage clamping circuit (e.g. clamping circuit 122 and 124) comprising first and second diodes (240 and 242) connected in antiparallel between a power supply line (Vdd core = 1.8 V at node 222 shown in fig. 3, and col. 4, lines 60-61) and a gate of the pass transistor (the gate of the pass transistor 234).

Regarding to claims 4, 5, Drapkin et al disclose an over-voltage protection circuit (fig. 1 and 3) comprises a pass transistor (234) having a first and a second current carrying terminals electrically connected to an input (input terminal 104) and an output signal line (the output node 114) respectively, a voltage clamping circuit (such as 122 and 124, shown in fig. 3, see col. 5, lines 59-61) that is electrically connected to a power supply line (Vdd core = 1.8V) and a gate of the pass transistor (234) and dynamically clamps a capacitively bootstrapped variable voltage at the gate of the pass transistor (234) within a first range so that the magnitudes of voltages across the pass transistor do not exceed a voltage in excess of about Vdd (e.g., see col. 5 and 6, lines 59-5) when Vin (Vdd pad = 3.3V) is equal to about 2Vdd (Vdd core = 1.8V), where Vin equals a voltage of an input supply and Vdd equals a power supply voltage on the power supply line (Vdd core).

Regarding to claim 7, Drapkin et al discloses the voltage clamping circuit (122 and 124) comprises first and second diodes (such as 240 and 242) electrically connected in series between the power supply and the gate of the pass transistor (206).

Regarding to claims 20, 21, 22, Drapkin et al discloses an over-voltage protection circuit (fig. 1 and 3) comprises a pass transistor (comprising 234) having a first and a second current carrying terminals electrically connected to an input (104) and an output signal line (the output node 110), a voltage clamping circuit (122 and 124, shown in fig. 3) that is electrically connected to a gate of the pass transistor (234) and is configured to clamp a bootstrapped voltage at the gate to a first voltage below a maximum voltage on the input line upon completion of pull-up and clamps the voltage at the gate to a

second voltage that is higher than a minimum voltage on the input line upon completion of a pull-down interval (e.g. see col. 5, lines 59-34).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drapkin et al in view of Partovi et al (USPN 5,576,635)

Regarding claims 13, 19, Drapkin et al disclose an over-voltage protection circuit (fig. 1 and 3) comprises first pass transistor (234) electrically connected between an input terminal (104) and an output terminal (the output node 114), a voltage clamping circuit (such as 122 and 124) comprising first and second diodes (such as 240 and 242) electrically connected in antiparallel between the power supply (Vdd core) and a gate of the first pass transistor (234). Drapkin et al do not disclose a second pass transistor is connected in parallel with the first transistor. Partovi et al disclose an over-voltage protection circuit (fig. 2) comprises a second pass transistors (110) having a gate coupled to a power supply (Vdd) and is connected in parallel with a first pass transistor (111). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modify the circuit of Drapkin et al with the second pass transistor as taught by Partovi et al in order to improve transient response (col. 9, lines 49-52).

5. Claims 2, 3, 6, 8-12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Drapkin et al in view of Kim (USPN 6,281,713). Drapkin et al disclose a voltage clamping circuit comprises MOS transistors configured as diodes (e.g. see col. 5, lines 59-64) which are connected in anti-parallel (e.g. see col. 5, lines 59-64) and a minimum voltage within the first range is equal to about Vdd – Vth1 (Vdd core – V-threshold of diode 242), wherein the Vth1 (V-threshold of diode 242) equals a threshold voltage of the first transistor. Drapkin et al do not disclose that the clamping transistors are NMOS transistors as claimed. Kim discloses a voltage clamping circuit (see fig. 6) comprises two clamping NMOS transistors (N61 and N62) and these transistors operates as anti-parallel connected diodes wherein a source of the first NMOS (N62) transistor is connected to a drain and a gate of the second NMOS transistor (N61), and a source of the second NMOS (N61) transistor is connected to a drain and a gate of the first NMOS transistor (N62) (see fig. 6 and col. 6, lines 24-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the clamping circuit of Drapkin et al to use NMOS antiparallel diodes as disclosed by Kim because Drapkin is silent about the type of MOS diodes used and Kim teaches that it is known to NMOS types (see col. 6, lines 40-45).

Regarding claims 10, 11 Drapkin et al disclose the voltage clamping circuit (122 and 124) and the pass transistor (234) drive the output signal line with an output signal having maximum positive voltage equal to about Vdd (Vdd core) for Vin (Vdd pad) greater than Vdd (e.g. see col. 6, lines 24-39 and col. 3, lines 38-46).

6. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drapkin et al in view of Partovi et al, and further in view of Kim. Drapkin et al and Partovi et al disclose all limitations of claim 13 except for the voltage clamping circuit comprises NMOS transistors as claimed. Kim discloses a voltage clamping circuit (see fig. 6) comprises two clamping NMOS transistors (N61 and N62) and these transistors operates as anti-parallel connected diodes wherein a source of the first NMOS (N62) transistor is connected to a drain and a gate of the second NMOS transistor (N61), and a source of the second NMOS (N61) transistor is connected to a drain and a gate of the first NMOS transistor (N62) (see fig. 6 and col. 6, lines 24-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the clamping circuit of Drapkin et al and Partovi use NMOS antiparallel diodes as disclosed by Kim because Drapkin and Partovi are silent about the type of MOS diodes used and Kim teaches that it is known to NMOS types (see col. 6, lines 40-45).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (703)-305-5988. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703)-308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-872-9318 for regular communications and (703)-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

DN

DN
December 15, 2003

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
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